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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/697,305	10/27/2000	Takaki Yoshida	YMOR:186	4222

7590 03/29/2005

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/697,305	YOSHIDA ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,53 and 59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8 and 19* is/are allowed.

6)☒ Claim(s) *1-7,9-18,20-22,53 and 59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/14/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 02/23/2005 have been fully considered but they are not persuasive.

The Applicant contends, "However, the reference at column 3, lines 56-57, and Fig. 2, explains that the document does not disclose a stuck-at-fault directory including physical layout information identifying physical sites on a physical layout of a semiconductor integrated circuit where a possible fault is likely to occur, as recited in applicants' claim 1".

The Examiner asserts that that Figure 2 is an algorithm for generating a fault list referred to as "final logical diagnostic list" (see Step 290 in Figure 2 of Balachandran) by pruning a larger fault list referred to as an "initial logical diagnostic list" (see Step 240 in Figure 2 of Balachandran). Col. 2, lines 27-30 in Balachandran teaches that the test analysis tool operable to create an initial logical diagnostic list of tested nets of the circuit associated with the potential stuck-at faults, hence the "initial logical diagnostic list" and the "final logical diagnostic list" are comprised of nets of the circuit associated with the potential stuck-at faults, the "final logical diagnostic list" being a pruned version of the "initial logical diagnostic list". Col. 6, lines 20-27 in Balachandran teaches that each net is identifiable based on a coordinate map, which may correspond to the physical dimensions of a particular circuit and at a minimum, should include the

horizontal and vertical dimensions and position of the net within circuit (Clearly these are physical dimensions associated with the circuit); hence a net is information identifying a physical site on a physical layout.

The Examiner asserts that Balachandran teaches a fault detecting method for a semiconductor integrated circuit (see Abstract in Balachandran; Note: Balachandran teaches that test patterns are applied to an integrated circuit to detect faults used in generating various diagnostic lists), comprising: providing a fault list comprising information identifying physical sites on a physical layout of a semiconductor integrated circuit where a possible fault is likely to occur (col. 2, lines 27-30 in Balachandran teaches that the test analysis tool operable to create an initial logical diagnostic list of tested nets of the circuit associated with the potential stuck-at faults, hence the "initial logical diagnostic list" and the "final logical diagnostic list" are comprised of nets of the circuit associated with the potential stuck-at faults, the "final logical diagnostic list" being a pruned version of the "initial logical diagnostic list"; col. 6, lines 20-27 in Balachandran teaches that each net is identifiable based on a coordinate map, which may correspond to the physical dimensions of a particular circuit and at a minimum, should include the horizontal and vertical dimensions and position of the net within circuit, clearly these are physical dimensions associated with the circuit; hence a net is information identifying a physical site on a physical layout), and information required to reduce faults (a fault list is information that can be used to reduce faults by providing fault information in the manufacturing or design phase so that corrective actions can be taken, such as;

replacing faulty circuitry with redundant circuitry, using error correcting codes, or discarding faulty IC chips during manufacturing, hence a fault list inherently corresponds to information required to reduce faults capable of being used throughout the life-cycle of the integrated circuit); and detecting faults in a semiconductor integrated circuit to which said fault list corresponds, said detecting in accordance with by said fault list (Step 220 in Figure 2 of Balachandran is a step for detecting faults in a semiconductor integrated circuit to which said stuck-at-fault dictionary fault list 100 corresponds, said detecting in accordance with by said stuck-at-fault dictionary fault list 100).

The Applicant contends, "Balachandran '830 does not disclose weighting". The Examiner disagrees and asserts that col. 6, lines 31-44 in Balachandran teach that if such a defect can cause a bridging fault between the two particular nets, the determination is weighted using the probability that a defect of that size exists to determine a final probability or ranking that particular bridging fault exists. The Authoritative Dictionary of IEEE Standards Terms defines weight a the values of a given digit position (for positional representations); hence ranking in the Balachandran patent is a means for weighting.

In response to applicant's argument that "According to Balachandran '830, it is 'impossible' to obtain fault coverage from a fault list, whereas the presently claimed invention makes it possible to obtain fault coverage by means of weighting, as the examples below show: ...", a recitation of the intended use of the claimed invention

must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963).

The Applicant contends, "Balachandran '830 does not disclose or suggest considering reliability data based on records of past use of cells or functional blocks of a semiconductor integrated circuit to which the fault list corresponds, and determining likelihoods of occurrence of defects based on the reliability data, as recited in applicants' claim 9".

The Examiner disagrees and asserts that, in Step 240 of Figure 2 of Balachandran, the "initial logical diagnostic list" is constructed based on actual prior test data performed in prior Steps 210-230; hence the "initial logical diagnostic list" is a record of past use of cells or functional blocks of a semiconductor integrated circuit to which the "final logical diagnostic list" corresponds. Col. 6, lines 31-44 in Balachandran teach that if such a defect can cause a bridging fault between the two particular nets, the determination is weighted using the probability that a defect of that size exists to determine a final probability or ranking that particular bridging fault exists; hence the "final logical diagnostic list" is ranked according to likelihoods of occurrence of defects based on the reliability data.

Regarding newly added claim 59. CFR §1.111(b) requires "The reply must present arguments pointing out the specific distinctions believed to render the claims, **including any newly presented claims**, patentable over any applied references. Since the Applicant presents no such arguments, the Examiner assumes that the Applicant believes that claim 59 is allowable for the same reasons as claim 9 from which it depends. The Examiner has presented arguments concerning claim 9, above. To summarize, Step 240 of Figure 2 of Balachandran, the "initial logical diagnostic list" is constructed based on actual prior test data performed in prior Steps 210-230; hence the "initial logical diagnostic list" is a record of past use of cells or functional blocks of a semiconductor integrated circuit to which the "final logical diagnostic list" corresponds. Col. 6, lines 31-44 in Balachandran teach that if such a defect can cause a bridging fault between the two particular nets, the determination is weighted using the probability that a defect of that size exists to determine a final probability or ranking that particular bridging fault exists; hence the "final logical diagnostic list" is ranked according to likelihoods of occurrence of defects based on the reliability data. The testing in Steps 210-230 comprises a number of past operations, a number of past defects. The constructed "initial logical diagnostic list" is reliability process status information concerning a number of process achievements for Steps 210-230.

The Examiner disagrees with the applicant and maintains all rejections of claims 1-7, 9-18, 20-22, 53 and 59. All amendments and arguments by the applicant have been

considered. It is the Examiner's conclusion that claims 1-7, 9-18, 20-22, 53 and 59 are not patentably distinct or non-obvious over the prior art of record in view of the references, Balachandran; Hari et al. (US 6618830 B1, hereafter referred to as Balachandran), Rohrbaugh, John G. et al. (US 6067651 A, hereafter referred to as Rohrbaugh), Allan; Gerard Anthony (US 6066179 A) and Agrawal; Prathima et al. (US 5257268 A, hereafter referred to as Agrawal) as applied in the previous office actions, filed 05/26/2004 and 11/29/2004. Therefore, the rejection is maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Balachandran; Hari et al. (US 6618830 B1, hereafter referred to as Balachandran). See the Non-Final Action filed 05/26/2004 for detailed action of prior rejections.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 2, 4-6, 9, 12-17, 20, 53 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balachandran; Hari et al. (US 6618830 B1, hereafter referred to as Balachandran) in view of Rohrbaugh, John G. et al. (US 6067651 A, hereafter referred to as Rohrbaugh).

See the Non-Final Action filed 05/26/2004 for detailed action of prior rejections.

35 U.S.C. 103(a) rejection of claim 53.

See the Final Action filed 11/29/2004 for detailed action of prior rejections.

35 U.S.C. 103(a) rejection of claim 59.

See rejection of claim 9 in the Non-Final Action filed 05/26/2004 for detailed action of prior rejections.

4. Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balachandran; Hari et al. (US 6618830 B1, hereafter referred to as Balachandran) and Rohrbaugh, John G. et al. (US 6067651 A, hereafter referred to as Rohrbaugh) in view of Allan; Gerard Anthony (US 6066179 A).

See the Non-Final Action filed 05/26/2004 for detailed action of prior rejections.

5. Claims 10, 11, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balachandran; Hari et al. (US 6618830 B1, hereafter referred to as Balachandran) and Rohrbaugh, John G. et al. (US 6067651 A, hereafter referred to as Rohrbaugh) in view of Agrawal; Prathima et al. (US 5257268 A, hereafter referred to as Agrawal).

See the Non-Final Action filed 05/26/2004 for detailed action of prior rejections.

Allowable Subject Matter

6. Claims 8 and 19 are allowed.

See the Non-Final Action filed 05/26/2004 for detailed action of prior rejections.

Conclusion

7. This is an RCE of applicant's earlier Application. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first

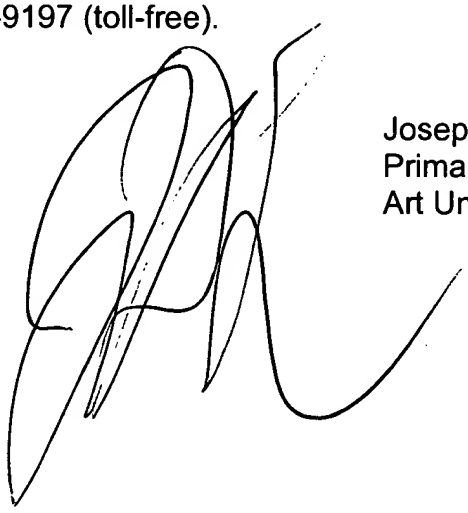
action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133